

# Michael E. Joyner C.I.D. +

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## Objective

To obtain technical management position with emphasis on Imaging or CAE/CAD design

## Summary of qualifications

Program manager. Schematic/verification/physical layout of mixed signal CMOS Imager designs. Certified PWB designer. Developed and administered documentation & process systems for technology company. Manage workgroups up to 20 people. Test & debug designs, and general engineering lab skills

## Professional experience

Sept. 1998 - Present Panavision Imaging, LLC., Homer NY  
(Originally: Photon Vision Systems, Inc, Silicon Video 2002, acquired by Panavision Dec.,2002)  
**Imager Design & Layout Engineer, Program Manager:** Company Founder (PVS). CAE design CMOS image/camera products for high volume consumer products (100,000+ per month), high res 4XHDTV, high end motion picture (movie making), prosumer, military, and industrial applications.

### Primary Management / Technical Duties:

- Program manager -sensor projects.
- CAD/CAE Department manger : Physical Layout- Silicon, PCB, Mechanical, other artwork/graphics
- CMOS Image sensor silicon design & layout, schematic entry, for 1.5um, 0.5, 0.35, and 0.18um processes.
- Full chip integration, Custom Analog, PLL, DACS, Distributed A/D, Pixels, Pitched Amplifiers, Discreet Amplifiers, Pitched Row Select Blocks, Highly Compacted Pitched Digital blocks, Pad frames & I/O. Area Array Sensors  $\geq 37$ mp, 14bit LVDS outputs, w/full onboard programmable timing. Linear Arrays  $\geq 32$ k, 12bit or Analog outputs, w/full onboard programmable timing.
- Calibre DRC, LVS verification, GDS Mask Tape Outs, Foundry submittal
- Develop / Review 3<sup>rd</sup> party PCB projects, and custom sensor packaging

### Other Management / Technical Duties:

- Assist in accessing customer requirements, feasibility, and specifications. Customer application support
- Marketing support- demo prep, graphics/artwork and trade show booth duties
- Documentation Manager (1998-2009): oversee & implement processes, procedures, documentation control, and training. (2009-Present) Sign off for engineering, and consult on ISO9001/documentation issues
- PCB design/layout.
- Mechanical- bond diagrams, package drawings, and data sheet supporting views/
- Electro Optical & debug testing, prototype/jig design & fixturing
- FPGA design

Jan. 1996 - Sept. 1998 Philips Broadband Networks, Manlius, NY

**Senior Printed Circuit Board Designer:** Design Printed Circuit Boards (multi-layer, thru-hole/SMT, double sided, auto-insertion), Schematic entry, Assembly drawings, Documentation, and etc. High volume DFM (design for manufacture), DFT (design for test), 850 MHz to 1 GHz designs. Products designed for cable TV, phone, and Internet delivery systems.

Aug. 1988 - Jan. 1996 CID Technologies, Liverpool, NY

**Engineering Specialist:** CAE/CAD design for CID imager based video cameras for use in military, industrial, aerospace, and radiation environment applications. FPGA/PGA/PAL design-implementation, schematic entry, simulation, PCB layouts. Prototyping - presentation quality. Engineering support (testing, calibration, documentation).

Mar. 1988 - Aug. 1988 Welch Allen, Skaneateles, NY

**Electromechanical Technician:** Temp professional. Build and repair medical & industrial endoscopes.

January 1980 - Mar. 1988 Syracuse Scientific, Clay, NY

**Engineering Technician:** Design electronic assemblies, and test fixtures for vidicon based video cameras used in medical x-ray systems. UL submittal documentation. Testing and prototyping to presentation level.

1979 - 1991 JK Systems, North Syracuse, NY

**Proprietor:** Design/modify/repair pro-audio & music equipment. Sub contracted to local merchants.

1985 - 1990 Syspec, Cicero, NY

**Consultant:** Design & repair of professional studio flash and audio equipment.

## Patents

**"A Video Bus For High Speed Multi-Resolution Imagers "** Zarnowski Jeffrey; Joyner Michael; Pace Matthew; Vogelsong Thomas, July-8-2003 Patent: US 6,590,198

**"A Video Bus For High Speed Multi-Resolution Imagers And Method Thereof"** Zarnowski Jeffrey; Joyner Michael; Pace Matthew; Vogelsong Thomas, October-14-2003 Patents: (US) 6,633,029 (China) PCT/US01/02309 (European) PCT/US02/01864, PCT/US01/02309 (Japan) 2001-553588 (Taiwan) 90101651

**"Scanning Image Employing Multiple Chips With Staggered Pixels"** Zarnowski; Jeffrey J.; Karia; Ketan V.; Joyner; Michael; Poonnen; Thomas, May-16-2006 Patent: US 7,045,758

**"Solid State Imager With Reduced Number Of Transistors Per Pixel"** Zarnowski; Jeffrey J.; Ambalavanar; Samuel D. ; Joyner; Michael; Karia; Ketan V. June-6-2006 Patent: US 7,057,150

**"Scanning imager employing multiple chips with staggered pixels"** Zarnowski; Jeffrey J.; Karia; Ketan V.; Joyner; Michael; Poonnen; Thomas, Oct-17-2006 Patent: US 7,122,778 Oct-31-2006 Patent: 7,129,461 June-30-2009 Patent: 7,554,067

**"Image Sensor ADC and CDS per Column"** Zarnowski; Jeffrey J.; Karia; Ketan V.; Joyner; Michael; Poonnen; Thomas, Mar-8-2011 Patent: US 7,903,159

**"Scanning imager employing multiple chips with staggered pixels"** Zarnowski; Jeffrey J.; Karia; Ketan V.; Joyner; Michael; Poonnen; Thomas; Liu; Li, Febr-22-2007 Patent Application Publication: US 2007/0040100 A1

**"Image sensor ADC and CDS per Column with Oversampling"** Zarnowski; Jeffrey J.; Liu; Li; Joyner; Michael; Karia; Ketan V., Feb-21-2008 Patent Application Publication: US 2008/0043128 A1

**"Sub-Pixel Array Optical Sensor"** Liu; Li; Zarnowski; Jeffrey J.; Karia; Ketan V.; Joyner; Michael; Poonnen; Thomas, Nov-26-2009 Patent Application Publication: US 2009/0290043 A1

**"Color Pixel Pattern Scheme for High Dynamic Range Optical Sensor"** Liu; Li; Zarnowski; Jeffrey J.; Karia; Ketan V.; Joyner; Michael; Poonnen; Thomas, Nov-26-2009 Patent Application Publication: US 2009/0290052 A1

**"Increasing The Resolution Of Color Sub-Pixel Arrays"** Zarnowski; Jeffrey J.; Karia; Ketan V.; Joyner; Michael; Poonnen; Thomas; Liu; Li, Jun-17-2010 Patent Application Publication: US 2007/0149393 A1

## Publications

Poonnen, T. Li Liu Karia, K.V. Joyner, M.E. Zarnowski, J.J. **"A CMOS video sensor for High Dynamic Range (HDR) imaging"** Panavision Imaging, LLC, Homer, NY,; 2008 42<sup>nd</sup> IEEE Asilomar Conference on Signals, Systems and Computers' Publication Date: 26-29 Oct.

R. M. Iodice, M. Joyner, C. S. Hong, D. Parker, Photon Vision Systems, Inc. **"Broadcast quality 3840 x 2160 color imager operating at 30 frames/s,"** Proc. SPIE Vol. 5017-01. Jan 2003 Santa Clara, CA.

Iodice, Robert M., Zarnowski, Jeffrey J., Pace, Matthew A., Joyner, Michael, Vogelsong, Thomas L., Zarnowski, Terry L., Photon Vision Systems, Inc., **"Ultrahigh-speed CMOS scanning linear imager family"**, Proc. SPIE Vol. 4306, p. 100-110 Jan 2001, San Jose, CA.

J. Zarnowski, M. Pace and M. Joyner, **"CMOS sensors overcome bad image and early hype"**, Laser Focus World, July 1999, Penwell.

J. Zarnowski, M. Pace and M. Joyner, **"1.5 FET per Pixel Standard CMOS Active Column Sensor"**, SPIE Vol. 3649-27, Jan 1999.

J. Zarnowski, B. Williams, M. Pace, M. Joyner, J. Carbone, C. Borman, F.S. Arnold, and Mark Wadsworth, **"Selectable One to Four Port Very, High speed 512 X 512 CID"**, SPIE, CCD and Solid State Optical Sensors Vol. 1447-18, February 1991, San Jose, CA.

**"Hills of Truxton"** ISBN 1-4196-0412-0 Apr. 2005 Booksurge publishing

**"Tales from the Turkey Woods"** ISBN 1-4392-0747-X Nov. 2008 Joyner Outdoor Media

**Professional memberships**

IPC Designers Council # 1021032:  
C.I.D. Interconnect Designer, Certified 1999 C.I.D.+ Advanced Certification 2006  
New York State Outdoor Writers Association- Active Member

**Education**

- Using Calibre, Mentor IC Layout - Mentor Graphics
- Rule Writing Calibre - Mentor Graphics
- Virtuoso XL Layout - Cadence
- Tanner EDA Tools 2000 - Tanner Corp.
- Practical Integrated Circuit Fabrication - Integrated Circuit Engineering (I.C.E.)
- PADS PWB Layout & Logic Schematic - Pads Corp.
- PWB Design - IPC Designers Council
- TQM ISO9000 - RIT
- Microsoft Excel, Word, Frontpage – Phillips Broadband
- AutoCad R13 - MicroCAD Managers
- Workview+ - ViewLogic Systems
- Xact DM - Xilinx Corp.
- Maxplus, PGA Design - Altera Corp.
- Design Techniques for Controlling Radiated Emissions - University of Wisconsin-Milwaukee
- EMI Compatibility Design Practices, System EMC - University of Wisconsin-Milwaukee
- Grounding/Shielding for Electronic Instrumentation - Missouri Rolla College
- Geometric Dimensioning and Tolerancing - Shepherd Industries
- Undergraduate Study 1981-1983 - Onondaga Community College
- Math/Industrial Arts Major 1978 - North Syracuse High-School

**Volunteer experience****Board of Directors:**

**NY State Chapter National Wild Turkey Federation** (1996-2005) President (2000-2004)

**Cortland Limbhangers Chapter, NWTF** (2000-2008) **Salt City Longspurs Chapter, NWTF** (1994-2009) President (1996-1998)

**CNY Chapter, Ruffed Grouse Society** (1995-2001) Vice President (1998-2001)

**Custom Call Makers and Collectors Guild** (2008-2009) President (2009)

**Race Course & Technical Director:**

**Race for the Cure @ Syracuse** (1995-1996), supervised 120+ volunteers.

**Chemical Bank Challenge @ Syracuse** (1993-1995), supervised 80+ volunteers

**Willow Bay Women's Distance Festival** (1994-present), supervise 20+ volunteers.

**Syracuse Festival of Races** (1993-1996), supervised 20+ volunteers.

**Hobbies**

Running (9 marathons), cycling, triathlons (half-ironman finisher), archery, hunting, and music

**References**

Available upon request