Michael E. Joyner C.I.D. +

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Objective

Obtain engineering management position with emphasis on Imaging or CAE/CAD design

Summary of qualifications

Design Bureau Principal. Program & CAE/CAD department manager. Schematic / verification / physical layout of mixed signal CMOS Imager designs. Certified PCB designer. Developed and administered documentation & process systems. Manage workgroups. Test & debug designs, optical & electronic engineering lab skills

Professional experience

Jan. 2013 – Present **President & Principle Engineer**

Town Line Technologies, LLC., Cortland NY: IC & PCB layout design services, testing services, program management, and consulting.

- 35 years of experience in the industry, extensive video background in consumer, medical, military, and machine vision markets,
- Prior experience in Vidicon / Plumicon Cameras, CID sensors & cameras
- 15 years designing CMOS image sensors with 40+ US and worldwide patents.
- Currently servicing 10-14 lyr rigid flex HD camera projects, large Xilinx / Altera BGA's, DDR2 etc. with 3g & 10g interfaces 3/3 & 4/4 rules. Mentor Pads ES suite of tools used for PCB design, Tanner EDA suite, Mentor Calibre for IC design

Sept. 1998 – Dec. 2012 **Co-founder**, **Imager Design & Layout Engineer, Program Manager**

Panavision Imaging, LLC., Homer NY (Orig. -Photon Vision Systems, acquired by Panavision Dec., 2002): CAE design CMOS image/camera products for high volume consumer products (100,000+ per month), high res 4XHDTV, high end motion picture (movie making), prosumer, military, and industrial applications.

Achievements:

- Produced physical layouts of all company sensor products with “first silicon” working die
- Physical layout and design input on ground breaking analog 60fps 8mp sensor in 2002
- Physical Layout and design input on a >120fps 37mp sensor in 2004
- Conceived product idea, physical Layout and design input for world’s first programmable, reconfigurable wide linear image sensor sold in volume production
- Mentored layout staff to successfully contribute layout work resulting in working first silicon.
- Resolved packaging issues with overseas vendor increasing yield from 68% to >88% on high volume linear sensor.
- Problem solving and research resulting in dozens of US and worldwide patents
- Conceived and implemented a documentation system that is efficient and requiring minimal overhead and unnecessary paperwork
- Facilitated implementation and adoption of ISO9001 policies achieving certification under 14 months

Primary Management / Technical Duties:

- Program manager -sensor projects.
- CAD/CAE Department manger : Physical Layout- Silicon, PCB, Mechanical, other artwork/graphics
- CMOS Image sensor silicon design & layout, schematic entry, for 1.5um to 0.18um process nodes/
- Full chip integration, Custom Analog, PLL, DACS, Distributed A/D, Pixels, Pitched Amplifiers/ Row Select Blocks/ Highly Compacted Pitched Digital blocks, Discreet Amplifiers, Pad frames & I/O. Area Array Sensors ≥ 37mp, LVDS >3GBs w/full onboard programmable timing. Linear Arrays.
- Calibre DRC, LVS verification, GDS Mask Tape Outs, Foundry submittal
- Develop / Review 3rd party PCB projects, and custom sensor packaging
- PCB design/layout. Mechanical dwg’s, and data sheet publishing / dwg’s / graphics.

Other Duties:

- Accessing customer requirements, feasibility, and specifications. Customer application support
- Marketing support- demo prep, graphics/artwork and trade show booth duties
- Documentation Manager: oversee & implement processes, procedures, documentation control, and training. Sign off for engineering, and consult on ISO9001/documentation issues
- Electro Optical & debug testing, prototype/jig design & fixturing

Jan. 1996 - Sept. 1998 **Senior Printed Circuit Board Designer**

Philips Broadband Networks, Manlius, NY: Design Printed Circuit Boards (multi-layer, thru-hole/SMT, double sided, auto-insertion), Schematic entry, Assembly drawings, Documentation, and etc. High volume DFM, DFT, 850 MHz to 1 GHz designs. Cable TV, and Internet delivery products.

Aug. 1988 - Jan. 1996 **Engineering Specialist**

CID Technologies, Liverpool, NY: CAE/CAD design for CID imager based video cameras for use in military, industrial, aerospace, and radiation environment applications. FPGA/PGA/PAL design-implementation, schematic entry, simulation, PCB layouts. Prototyping - presentation quality. Eng. support (testing, calibration, documentation).

Jan. 1980 - Mar. 1988 **Engineering Technician**

Syracuse Scientific, Clay, NY: Design electronic assemblies / test fixtures for vidicon based video cameras used in medical x-ray systems. UL submittal documentation. Testing and prototyping to presentation level.

Jan. 1977 - Dec. 1991 **President, Owner**

JK Systems, North Syracuse: New York Design, modify, and repair pro-audio/music equipment. Authorized repair for Mesa Boogie Amplifiers. Sub contracted to local merchants.

Sept. 1978 - Jan. 1980 **Engineering Technician**

Kipco & Omnetics, Clay, NY: Design & Prototype electronic assemblies & test fixtures, testing for industrial motor & lighting control products. Testing and prototyping to presentation level.

Patents

"A Video Bus For High Speed Multi-Resolution Imagers " July-8-2003 Patent: US 6,590,198

"A Video Bus For High Speed Multi-Resolution Imagers And Method Thereof" October-14-2003 Patents: (US) 6,633,029 (China) PCT/US01/02309 (European) PCT/US02/01864, PCT/US01/02309 (Japan) 2001-553588 (Taiwan) 90101651

“Scanning Image Employing Multiple Chips With Staggered Pixels” May-16-2006 Patent: US 7,045,758

"Solid State Imager With Reduced Number Of Transistors Per Pixel" June-6-2006 Patent: US 7,057,150

“Scanning imager employing multiple chips with staggered pixels” Oct-17-2006 Patent: US 7,122,778 Oct-31-2006 Patent: 7,129,461 June-30-2009 Patent: 7,554,067, EP1878215 B1

“Image Sensor ADC and CDS per Column” Mar-8-2011 Patent: US 7,903,159, CA2758275A1, CN102461158A, EP2417763A1

“Sub-Pixel Array Optical Sensor” Oct-11-2011 Patent: US 8,035,711

“Image sensor ADC and CDS per Column with Oversampling” May-1-2012 Patent: US 8,169,517, CA2758275A1, CN102461158A, WO2010117462A1

“Color Pixel Pattern Scheme for High Dynamic Range Optical Sensor” Nov-26-2009 Patent Application: US 2009/0290052 A1

“Increasing The Resolution Of Color Sub-Pixel Arrays” Jun-17-2010 Patent Application: US 2007/0149393 A1, EP2540077A1, WO2011106461A1

“Variable Active Image Area Array Sensor” Aug-25-2011 Patent Application: WO 2011106461 A1, US 2011/0205384 A, CA2790853 A1, EP2539854A1

“Image sensor adaptive column readout structure” Sep-14-2011 Patent Application: PCT/US2012/055575, WO2013040458 A1

Publications

“A CMOS video sensor for High Dynamic Range (HDR) imaging,“ 2008 42nd IEEE Asilomar Conference on Signals, Systems and Computers’ Publication Date: 26-29 Oct.

“Broadcast quality 3840 x 2160 color imager operating at 30 frames/s,” Proc. SPIE Vol. 5017-01. Jan 2003 Santa Clara, CA.

“Ultrahigh-speed CMOS scanning linear imager family,” Proc. SPIE Vol. 4306 Jan 2001, San Jose, CA.

“CMOS sensors overcome bad image and early hype”, Laser Focus World, July 1999, Penwell.

“1.5 FET per Pixel Standard CMOS Active Column Sensor”, SPIE Vol. 3649-27, Jan 1999.

“Selectable One to Four Port Very, High speed 512 X 512 CID”, SPIE, CCD and Solid State Optical Sensors Vol. 1447-18, February 1991, San Jose, CA.

Publications (other)

"Grand Days in the Turkey Woods" ISBN 1-5001-1281-X Aug. 2014 Joyner Outdoor Media

"Tales from the Turkey Woods" ISBN 1-4392-0747-X Nov. 2008 Joyner Outdoor Media

"Hills of Truxton" ISBN 1-4196-0412-0 Apr. 2005 Booksurge publishing

"Syracuse Ironman 70.3 & Other Ironman Journey's" Blog **syracuseironman.wordpress.com**

Professional memberships

- IPC Designers Council # 1021032:
- IEEE Member - #92567483
- SPIE Member - #350208
- New York State Outdoor Writers Association- Active Member

Education

- Using Calibre, Mentor IC Layout/ Rule Writing - Mentor Graphics • Virtuoso XL Layout - Cadence
- Tanner EDA Tools 2000 - Tanner Corp
- Practical Integrated Circuit Fabrication - Integrated Circuit Engineering (I.C.E.)
- IPC Certified Interconnect Designer - C.I.D., Certified 1999 C.I.D.+ Advanced Certification 2006
- PADS PWB Layout & Logic Schematic - Pads Corp. • PWB Design - IPC Designers Council
- AutoCad R13 - MicroCAD Managers • TQM ISO9000 - RIT
- Microsoft Excel, Word, Frontpage – Phillips Broadband
- Workview+ - ViewLogic Systems • Xact DM - Xilinx Corp. • Maxplus, PGA Design - Altera Corp.
- Design Techniques for Controlling Radiated Emissions - University of Wisconsin-Milwaukee
- EMI Compatibility Design Practices, System EMC - University of Wisconsin-Milwaukee
- Grounding/Shielding for Electronic Instrumentation - Missouri Rolla College
- Geometric Dimensioning and Tolerancing - Shepherd Industries
- Undergraduate Study 1981-1983 - Onondaga Community College
- Math/Industrial Arts Major 1978 - North Syracuse High-School

Volunteer experience

Board of Directors:

- New York Outdoor Writers Assoc. (NYSOWA) VP- Western & CNY Regions (2014-current)
- NY State Chapter National Wild Turkey Federation (1996-2005) President (2000-2004)
- Cortland Limbhangers Chapter, NWTF (2000-2008)
- Salt City Longspurs Chapter, NWTF (1994-2009) President (1996-1998)
- CNY Chapter, Ruffed Grouse Society (1995-2001) Vice President (1998-2001)
- Custom Call Makers and Collectors Guild (2008-2009) President (2009)

Race Course & Technical Director:

- Willow Bay Women's Distance Festival (1994-present), supervise 20+ volunteers.
- Race for the Cure @ Syracuse (1995-1996), supervised 120+ volunteers.
- Chemical Bank Challenge @ Syracuse (1993-1995), supervised 80+ volunteers
- Syracuse Festival of Races (1993-1996), supervised 20+ volunteers.

Hobbies

Running (9 marathons), cycling, triathlons (2 half-ironmans), archery, hunting, and music